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| 466 | 7590 07/27 | 2004 | | | EXAM | INER |
| YOUNG & THOMPSON | | | | | LUU, CHUONG A | |
| 745 SOUTH 23RD STREET 2ND FLOOR ARLINGTON, VA 22202 | | | | ART UNIT | PAPER NUMBER | |
| | | | | | 2825 | |

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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|---|---|--|--|--|--|--|--|
| | Application No. | Applicant(s) | | | | | |
| | 09/715,000 | AOKI ET AL. | | | | | |
| Office Action Summary | Examiner | Art Unit | | | | | |
| | Chuong A Luu | 2825 | | | | | |
| The MAILING DATE of this communic Period for Reply | cation appears on the cover sheet with | h the correspondence address | | | | | |
| A SHORTENED STATUTORY PERIOD FOTHE MAILING DATE OF THIS COMMUNION. - Extensions of time may be available under the provisions of after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30 If NO period for reply is specified above, the maximum states are reply within the set or extended period for reply within the set or extended period for reply any reply received by the Office later than three months after earned patent term adjustment. See 37 CFR 1.704(b). | CATION. of 37 CFR 1.136(a). In no event, however, may a rejunication.) days, a reply within the statutory minimum of thirty utory period will apply and will expire SIX (6) MONT will, by statute, cause the application to become ABA | ply be timely filed (30) days will be considered timely. HS from the mailing date of this communication. INDONED (35 U.S.C. § 133). | | | | | |
| Status | | | | | | | |
| 1)⊠ Responsive to communication(s) filed | d on 11 March 2004. | • | | | | | |
| | b)⊠ This action is non-final. | | | | | | |
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| Disposition of Claims | | | | | | | |
| 4) | e withdrawn from consideration. 6 is/are rejected. | | | | | | |
| Application Papers | | | | | | | |
| 9) ☐ The specification is objected to by the | Examiner. | | | | | | |
| 10) The drawing(s) filed on is/are: | a) ☐ accepted or b) ☐ objected to b | y the Examiner. | | | | | |
| Applicant may not request that any object | tion to the drawing(s) be held in abeyand | e. See 37 CFR 1.85(a). | | | | | |
| Replacement drawing sheet(s) including 11) The oath or declaration is objected to | | | | | | | |
| Priority under 35 U.S.C. § 119 | | | | | | | |
| 12) Acknowledgment is made of a claim for a) All b) Some * c) None of: 1. Certified copies of the priority of the certified copies of the copies of the priority of the certified copies of the certified copies of application from the Internation * See the attached detailed Office action | locuments have been received. locuments have been received in Ap of the priority documents have been re al Bureau (PCT Rule 17.2(a)). | plication No eceived in this National Stage | | | | | |
| Attachment(s) | _ | | | | | | |
| Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PT | 4) Interview Su | mmary (PTO-413) /Mail Date | | | | | |
| Notice of Draftsperson's Patent Drawing Review (PT3) Information Disclosure Statement(s) (PTO-1449 or F Paper No(s)/Mail Date 1/27/2003. | | ormal Patent Application (PTO-152) | | | | | |

Art Unit: 2825

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-3, 7-19, 21, 24-33 and 57-66 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTION

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1-3, 11, 13, 16, 18-19, 27, 29, 32 and 57-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohashi et al. (U.S. 6,376,345 B1) in view of Ngo et al. (U.S. 6,596,631 B1).

Ohashi discloses a method for forming a semiconductor device with Respect to claims:

(1) simultaneously or subsequently carrying out an anti-corrosion treatment by exposing said surface of said semiconductor substrate to a solution containing an anti-corrosive agent (see column 16, lines 1-16);

subsequently, separately forming a copper-diffusion stopper insulating film (43) over said surface of said semiconductor substrate (see Figures 10-11);

- (2) wherein said surface of said semiconductor substrate includes at least one of a copper interconnection, a copper based interconnection and a copper alloy interconnection which are formed in a damascene method (see column 15, lines 60-61);
- (3); (19) wherein said anti-corrosion treatment is carried out in a cleaning process after a chemical mechanical polishing process is carried out to said surface of said semiconductor substrate (see column 16, lines 1-16);
- (11); (27) wherein a plurality of said five-membered hetero-cyclic compound comprise benzotriazole, (see column 16, lines 1-16);
- (13); (29) wherein said anti-corrosive agent comprises at least one of aromatic compounds having benzene-rings and derivatives thereof (see column 16, lines 1-16);
- (16) (32) wherein said copper-diffusion stopper insulating film comprises an SiN film (see column 14, lines 39-40);
- (18) carrying out a chemical mechanical polishing process for forming said at least interconnection in at least a groove in said semiconductor substrate (see Figures 10-11);

simultaneously or subsequently carrying out an anti-corrosion treatment by exposing a surface of said semiconductor substrate to a solution containing an anti-corrosive agent (see column 16, lines 1-16);

subsequently, separately forming a copper-diffusion stopper insulating film (43) over said surface of said semiconductor substrate (see Figures 10-11);

Art Unit: 2825

(57); (60) wherein said step of carrying out an anti-corrosion treatment comprises flows the anti-corrosive agent onto the surface of the substrate (see column 16, lines 1-16);

- (58); (61) wherein said step of forming a insulating film comprises forming an insulating film by chemical vapor deposition (see column 14, lines 39-42);
- (59); (62) wherein the copper-diffusion stopper insulating film comprises one of SiN film (see column 14, lines 39-40);
- (63) simultaneously carrying out an anti-corrosion treatment by exposing said surface of said semiconductor substrate to a solution containing an anti-corrosive agent (see column 16, lines 1-16);

subsequently, separately forming a copper-diffusion stopper insulating film (43) over said surface of said semiconductor substrate (see Figures 10-11);

(64) wherein said semiconductor substrate has at least one interconnection made of a metal selected from the group consisting of copper, copper-based materials, and copper alloys, and said method further comprising the step of carrying out a chemical mechanical polishing process for forming at least one interconnection in at least one groove in said semiconductor substrate prior to said removing metal contaminations step (see column 13, lines 26-35. Figures 10-11);

Ohashi teaches the above outlined features except for removing CuO_x from said surface using a cleaning solution; wherein said step of removing CuO_x comprises rotating said semiconductor substrate while applying a cleaning solution; further comprising the step of removing particle contaminations prior to said step of removing

Application/Control Number: 09/715,000

Art Unit: 2825

CuO_x. However, Ngo discloses a method for manufacturing copper interconnect capping layers with (1); (18); (63)... removing CuO_x from said surface substrate using a cleaning solution (see column 8, lines 19-25); (65) wherein said step of removing CuO_x comprises rotating said semiconductor substrate while applying a cleaning solution (see column 5, lines 58-64); (66) further comprising the step of removing particle contaminations prior to said step of removing CuO_x.(see column 5, lines 1-10).

Therefore, it would have been obvious to one skilled in the art at the time of claimed invention to combine Ngo's teaching into Ohashi's process for removing copper oxide layer. Doing so, it would increase the adhesion of the capping layer and reduce corrosion and/or poisoning of the copper and capping layer interface of the semiconductor interconnect structure.

Claims 8-10, 14, 24-26 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohashi et al. (U.S. 6,376,345 B1) in view of Ngo et al. (U.S. 6,596,631 B1) and further in view of Lawson (U.S. 4,978,756)

Ohashi and Ngo teach everything above except for using specific chemical compounds and concentrations for corrosive treatment and cleaning procedures.

However, Lawson discloses compounds can be used for the treatment of metal (8);

(24) wherein said anti-corrosive agent comprises at least one of hetero-cyclic compounds and derivatives thereof; (9); (25) wherein said anti-corrosive agent comprises at least one selected from the groups consisting of four-membered hetero-cyclic compounds having two nitrogen atoms, five-membered hetero-cyclic

compounds having three nitrogen atoms, six-membered hetero-cyclic compounds having three nitrogen atoms and derivatives thereof; (14); (30) wherein said aromatic compounds having benzene-rings comprise gallic acids and tannic acids; (10); (26) wherein one of said four-membered hetero-cyclic compounds comprises indazole (see column 1, lines 4-8, lines 9-11; column 2, lines 5-66; column 3, lines 28-57; column 4, lines 4-44; column 7, lines 48-58; column 17, lines 10-50; and column 18, lines 57-68). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above teachings by apply certain chemical compounds and concentration to manufacture a semiconductor interconnection to enhance the performance of semiconductor device.

Claims 7 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over over Ohashi et al. (U.S. 6,376,345 B1) in view of Ngo et al. (U.S. 6,596,631 B1) and further in view of Admitted Prior Art (hereinafter APA)

Ohashi and Ngo disclose everything above but fails to apply cleaning solution comprises a carboxylic acid. However, APA discloses a method for improving wafer surface with (7); (21) wherein said cleaning solution comprises a carboxylic acid based cleaning solution (see page 3, lines 1-5). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above teachings by apply certain chemical compounds to clean a semiconductor interconnection during manufacture a semiconductor device. Doing so would facilitate the manufacture of an interconnection and increase the contacting area.

Art Unit: 2825

Claims 12, 15, 17, 28, 31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohashi et al. (U.S. 6,376,345 B1) in view of Ngo et al. (U.S. 6,596,631 B1).

Ohashi and Ngo disclose the claimed invention except for using SiON film as copper-diffusion stopper insulating film material; wherein said at least one of gallic acids and tannic acids, anti-corrosion agent is contained in the range of 1 ppm to 5%. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Avanzino by selecting SiON film as copper-diffusion stopper insulating film material and the concentration of gallic acids, tannic acids and anti-corrosion agent, which is a well-known material in the semiconductor industry, since it has been held to be within the general skill of a worker in the art to select a known material and concentration of chemicals on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Application/Control Number: 09/715,000

Art Unit: 2825

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 26, 2004

Page 8